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Use of Fault-Resistant Distributed Computation Systems for Power Systems Control

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1 INTRODUCTION

During last decade significant progress in computation systems' hardware and software development has been signed. This fact correspondingly results in change of approaches for power units control systems architecture.

It should be noticed that today power units control systems including digital substations, are built without accounting distributed computations option. More attention is usually paid for data acquisition task. Moreover, traditional ways of elements interconnections reliability provision have a set of special features, which will be turned into disadvantages in case of digital substations mass use.

Let's review methodological experience, modern approaches for distributed computation systems (CS) development and also perspectives of their use in power units control systems.

2 USE OF DISTRIBUTED CS FOR POWER UNITS CONTROL

2.1 Generalities

For wide range of power units control tasks the characteristic feature is the need for faultless operation and high processing speed of control system. One of the perspective approaches is to use computation systems with programmable structure (PS) for solving tasks of such class.

Survivability is CS's ability to use in any moment summary capacity of all operable elementary computers (EC) for solving tasks (under notion EC we understand a separate microprocessor device). The affinity of CS survivability is provided by program orientation of its structure and its components functional interaction. It is clear that in survivable CS calculation resources are used quite more effectively, than in CS with structural redundancy (e.g. in CS with reservation or majorization). EC failures lead to reduction of CS productivity. In this connection survivable CS may have two possible ways of computations restoration.

In first case, when it is important to solve a task in full volume and its solving time is not very important, general computational load remains. Computational load of each operable EC rises and task solving time decreases, so productivity degradation takes place.

In second case when a task has to be solved during a set time interval, in spite of solution quality decrease, the calculations are restored partially. In his situation computational resources redistribution is done for solving tasks of higher priority. Electric power systems (EPS) control is related exactly to this type of tasks. Such tasks adaptation during EC breakdowns can be made for example by increasing number of processor cycles given to tasks in accordance with priority of the

task. To be exact, in order to save the highest priority tasks computation speed during faults we have to sacrifice the quality of lower priority tasks computation by increasing their allowable solving time.

Research in this direction are been conducted during long time. So, in the middle of 1980-s a specialized distributed operation system MICROS [1-3] has been developed. Its purpose was to combine high-efficient parallel task solving mode and services provided by computer networks.

As architectural decisions used in microprocessor computational systems constantly developing, approaches used for programmable structure computational systems building are also change.

2.2 Modern approaches for distributed computation systems design

During last decade means of computation available for needs of industrial automation have came through substantial changes, which touched first of all:

- basic electronic elements and microprocessor devices reliability;
- microprocessor devices capacity and means of its provision;
- network capacity of interfaces used for data exchange between units;
- production cost.

From viewpoint of distributed computation systems one of the very important points was appearance of available multiprocessor microprocessor devices.

There are following variants of multiprocessor systems architecture:

- use of specialized motherboards, allowing installation of 1 to 4 separate processors;
- integration of several processor crystals into one device;
- combination of several microprocessor cores in one crystal.

The last architectural approach is also interesting because it provides maximal network capacity while data exchange between cores. This allows solving parallel tasks more effectively due to reduction of overhead charges for data exchange between parallel processes. It should be noticed that during last several years an idea of using graphical processors for computations is developing rapidly. Graphical processors are able of integrating up to several hundreds processor cores in one crystal. While developing this architecture the greatest attention was paid for problems of large data arrays parallel processing organization.

No less important points are:

- network adapters speed increase up to 1000 M bit/sec, which allows reducing data exchange time between devices.
- number of network adapters installed directly in motherboards increase.

In this connection, it should be noticed:

1. The task of specified computation capacity provision using task distribution between several microprocessor devices loses its urgency because of significant and stabile growth of these devices productivity, which is provided by constant clock frequency increase and architectural decisions evolution: use of conveyers, branching and operation forecast algorithms, intermediate fast memory, microprocessor cores number growth;
2. The question of applied problem solution process parallelization in one microprocessor device is still relevant (in this case minimal overhead charges for data exchange between parallel processes are provided). Study of graphical processors use for power engineering problems possibility is of special interest;
3. Despite of significantly grown technical devises reliability the problem of CS reliability is still relevant. CS reliability can be provided both at the expense of survivability affinity (task redistribution between CS microprocessor units), and at the expense of structural redundancy (backup of microprocessor units responsible for interaction with controlled object).

Taking into account aforesaid, in [4] approaches for fault-resistant power systems control CS software development are defined. Now let's review approaches for reliable connection between elements of such CS organization.

2.3 Approaches for organization of communication networks between distributed CS elements

Due to mass microprocessor devices introduction for modern power units control systems there is a tendency of transition from separate units, indirectly connected with each other by controlled object or by principle of operation (for example, relay protection and anti-fault automation systems boxes are installed into one same terminal of a substation) to their integration into united network with

purpose of data acquisition and control. In this case connection between devices on physical layer is made as a rule on the basis of bus architecture. In recent time Industrial Ethernet becomes to be more and more popular in this area.

A tendency of transition to completely digital substations has occurred. In this case both measured values and commands to execution units will be transmitted through digital network in real time mode. In fact, digital substation communication network is active element of control loop, and this determines increasing demands on reliability and processing speed. Particularly, reliability demands, analogical to ones for relay protection and anti-fault automation devices have to be applied for active network equipment at a digital substation.

On physical layer reliability is provided usually by bus doubling or redundant rings organization. Nevertheless, traditional approaches for communication network reliability provision have a number of obvious drawbacks:

1. Big number of additional active equipment in control loop used only for network communication organization.
2. Significant complication of system exploitation due to necessity of network infrastructure maintenance.
3. Necessity of IT-specialists service for control loop devices maintenance.

An approach when communication network (and microprocessor devices interconnected by this network) is a part of distributed CS with programmable structure seems to be more prospective. Such an approach has following advantages over traditional ones:

1. Use of additional active network equipment is eliminated or minimized, depending on the topology has been chosen.
2. Communication lines are laid directly between microprocessor devices according to the network topology has been chosen.
3. The information packets commutation function is implemented by microprocessor device itself like one of technological functions which minimizes possibility of supernumerary behavior of network communication. On physical layer this option is provided by equipping device with necessary number of network adapters (see 2.2).
4. Highly skilled IT-personnel are not necessary for communication network maintenance because all maintenance operations are reduced to devices cable connections checking.

There are certain methodologies for network connection structure choice which provides specified CS reliability. Let's make their detailed review:

Under notion of distributed CS structure we understand a **G**-graph which nodes are associated with elementary computers (in this case – power unit control microprocessor devices), and ribs are associated with connection lines between them [5]. While forming CS structures following demands have to be taken into account:

1. Provision of effective information exchange between computers at large number of devices in condition of full graph interconnections (fully intermeshed exchange, “each-with-each”) realization impossibility, as because fully connected graph is very hard to realize technically and consequently is economically ineffective.
2. Provision of expansion easiness and devices' number reduction.
3. Provision of structure homogeneity and devices uniformity.

As structures meeting presented demands we can single out **L(N,v,g)**-graphs. This is an undirected graph with number of nodes **N** and node orders **v** respectively and circumference magnitude (shortest simple cycle length) **g**. In **L(N,v,g)**-graphs each node at $v \geq 3$ belongs to **v** shortest simple cycles with length **g**. At $v=2$ **L**-graph is a simple cycle with **N** nodes which corresponds to CS ring structure. **L**-graphs, which have minimal **d** diameter and consequently minimal transmission data delay, are called optimal. In figure 1 examples of optimal **L(8,3,4)** and **L(8,4,4)**-graphs are presented.

During the study of correlation between CS structural survivability and number of nodes **v** in each computer, conducted in the context of project MICROS in USSR Academy of Sciences, Siberian Branch, and then proceeded in Russian Academy of Sciences, Siberian Branch, it has been found that operable system devices connectivity probability high meanings in case of their failure and in case of lines failure could be reached as already as $v=4$ [5]. Therefore, in order to build a distributed CS providing reliable connection between its elements, two- or three- or four-polar elementary computers will be enough.

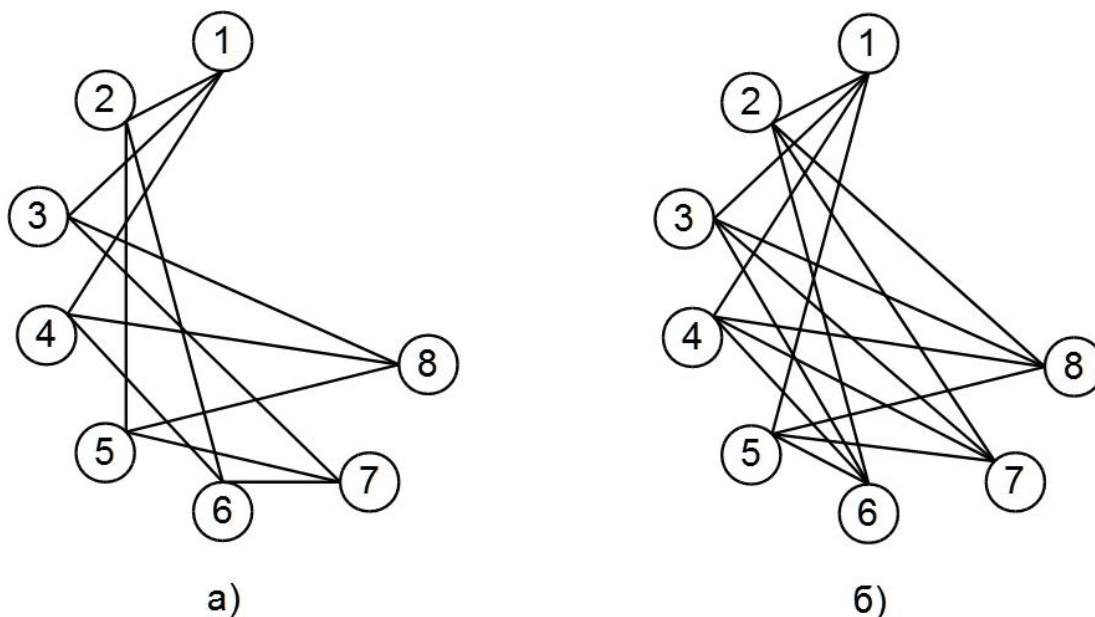


Fig. 1: Examples of optimal L-graphs: a – $L(8,3,4)$ -graph, b – $L(8,4,4)$ -graph

In the context of power unit control task while distributed CS structure choice it should be taken into account possible failure of simultaneously few devices (while scheduled operations or equipment failure, etc.). In connection with it, it is reasonable to eliminate from the consideration $L(N,2,g)$ -graphs and ring schemas corresponding to them, because failure of any two devices in such system will irreversibly destruct its connectivity. It is also necessary to take into account that graph connectivity may be interrupted at simultaneous failure of devices adjacent with given device. For example, in case of any three adjacent devices failure, connectivity of graph in **figure 1.a** will be interrupted irreversibly and in case of four adjacent devices failure connectivity of graph in **figure 1.b** will be interrupted. Therefore while choosing CS structure it seems appropriate to use $L(N,4,g)$ -graphs. At large number of system devices, use of $L(N,3,g)$ -graph based schemas can be recognized admissible in order to minimize number of cable connections.

3 CONCLUSION

Taking into account substantial changes in industrial automatics computation devices market that took place during last 10 years, the approaches for power unit control systems design also changed. Special attention should be paid for task of reliable connection between control system microprocessor devices organization.

In comparison with traditional ways of solving this problem, an approach when communication network (and microprocessor devices interconnected by it) is a part of distributed computation system with programmable structure seems to be most prospective. In the context of presented approach there are methodologies of connection network structure choice, allowing both optimal reliability and optimal operation speed. From this viewpoint it is reasonable to build network structure on the basis of $L(N,4,g)$ -graphs.

In case of creating power unit control system on the basis of distributed computation system with programmable structure there is an opportunity not to simply provide data exchange reliability between controlling microprocessor devices, but also significantly raise control system reliability at the expense of redistribution of tasks between them.

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